

CBCS SCHEME

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15EC745

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020 CAD for VLSI

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing full question from each module.

Module-1

- 1 a. Briefly explain the different algorithms for NP hard problems. (08 Marks)
b. Discuss the three main search techniques used in graph search algorithm. (08 Marks)

OR

- 2 a. Explain line sweep method with the help of an algorithm. (10 Marks)
b. Write shortest path algorithm. (06 Marks)

Module-2

- 3 a. Write notes on: i) Linked list ii) Corner stitching. (08 Marks)
b. Briefly explain the relationship between different graph classes of physical design. (08 Marks)

OR

- 4 a. List out and explain the various atomic operations supported by layout editor. (10 Marks)
b. Explain multilayer operations with the help of a neat diagram. (06 Marks)

Module-3

- 5 a. Briefly explain design style specific partitioning problems. (06 Marks)
b. Explain the classification of floorplanning algorithms. (10 Marks)

OR

- 6 a. Explain the classification of partitioning algorithms. (06 Marks)
b. What are the various factors to be considered by the chip planning, floorplanning, pin assignment and placement algorithms. (10 Marks)

Module-4

- 7 a. Classify the pin assignment algorithms and explain briefly. (10 Marks)
b. Explain the classification of placement algorithms. (06 Marks)

OR

- 8 a. Write a short note on sequence pair technique. (06 Marks)
b. Explain the various objective functions and placement procedures in Breuer's algorithm. (10 Marks)

Module-5

- 9 a. Explain design style specific global routing problems. (06 Marks)
b. What are the various parameters to be considered in detailed routing problem? Also define detailed routing. (10 Marks)

OR

- 10 a. Write an algorithms for LEE – ROUTER. (06 Marks)
b. Briefly explain five distinct phases decomposing MPCB routing problem. (10 Marks)

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